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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,851	07/25/2001	Hak Su Kim	CIT/K-152	3915

34610 7590 03/12/2003

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER

LESPERANCE, JEAN E

ART UNIT PAPER NUMBER

2674

DATE MAILED: 03/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

11

Office Action Summary

Application No.

09/911,851

Applicant(s)

KIM, HAK SU

Examiner

Jean E Lesperance

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6 and 7 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, and 7 are rejected under 35 U.S.C. 102 (b) as being unpatentable over U.S. Patent # 5,532,712 ("Tsuda et al.").

As for claim 1, Tsuda et al. teach an insulated DC-Dc converter 11 outputs a +5 VDC signal Vdd1 for generating a logic signal (column 8, lines 64-65) including in the switching device 7 corresponding to a DC-DC converter provided inside one chip, for controlling an external voltage input depending on a timing control signal and providing a controlled DC voltage; the PC terminal is connected through an inverter 3cto a first input of each of the plurality of gate circuits 2b (column 6, lines 64-66) corresponding to an interface unit provided inside the chip, for interface with parts outside the chip; shift register Fig.8 (3a) corresponding to a memory provided inside the chip, for storing display information transmitted through the interface unit: latch Fig.8 (3b) corresponding to a data processor provided inside the chip, for providing a display data to a display panel of the EL display device using the display information stored in the memory and

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the controlled DC voltage output from the DC-Dc converter; a plurality of first gate circuits 2a and a plurality of second gate circuits 2b (Fig.8) corresponding to a scan processor provided inside the chip, for outputting scan data to the display panel using the display information and the controlled DC-voltage output from the DC-DC converter: and the clock terminal connected to the latch 6b and through an inverter 3e to the shift register 3a (column 7, lines 38-39) corresponding to a timing control unit provided inside the chip, for providing the timing control signal to the DC-DC converter, the interface unit, the memory, the data processor, and the scan processor.

As for claim 2, Tsuda et al. teach a power supply terminal not shown in Fig.12, a positive voltage +V as a signal Vdd2 is supplied to a first terminal of the switch SW1 (column 10, lines 15-17) corresponding to power peripheral unit provided outside the chip, for controlling input and output voltages of the DC-DC converter, preventing a backward current from occurring during the DC-DC conversion, and maintaining the input DC voltage for a predetermined-time.

As for claim 3, Tsuda et al. teach an insulated DC-DC converter (Fig.10) where it is inherent to include an inductor, a diode, and a resistor.

As for claims 6 and 7, Tsuda et al. teach a positive voltage +V as a signal Vdd2 is supplied to a first terminal of the switch SW1 (column 10, lines 15-17) corresponding to generating a DC voltage; Fig.16 are timing charts showing the relation between voltage changes across the electrodes of the pixels and the state changes of the operation signals (column 11, lines 13-16) corresponding to generating a voltage control signal in response to a timing control signal: the switching circuit 100 of the liquid crystal

display device accords with so-called $\frac{1}{2}$ bias drive method, when the absolute value of the voltage across the two electrodes of a respective one of the pixels G1 to G4 becomes twice the supply voltage V (column 10, lines 51-55) corresponding to generating an impedance value corresponding to the voltage control signal; the insulated DC-DC converter distribute a +5 Vdd (Fig.10) distributing the DC voltage by the resistor and the impedance value; and Vdd2 and Vss are new voltage distributed by the insulated DC-DC converter (Fig.10) corresponding to generating a new DC voltage using the distributed voltage.

Allowable Subject Matter

3. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

4. The following is an examiner's statement of reasons for allowance:

None of the references either singularly or in combination, teaches or fairly suggests: The driving circuit for an organic EL device, wherein the power peripheral unit includes: an input terminal providing an applying external voltage an external voltage to the DC-DC converter; an output terminal output terminal outputting the controlled DC voltage output from the DC-DC converter to the outside the chip; a first capacitor connected with the input terminal in parallel to minimize fluctuation of the input voltage;

a second capacitor connected with the output terminal in parallel to minimize fluctuation of the controlled DC voltage; an inductor connected in series between the input terminal and the output terminal, for maintaining the external voltage applied to the DC-DC converter for a predetermined time; and a diode connected in series between the input terminal and the output terminal, for preventing a backward current from occurring.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tsuda et al. teach a drive circuit for use with a transmissive scattered liquid crystal display device, prevents a residual image caused by a high speed display switching, while having a reduced size and fewer parts, thereby improving reliability. The output of the buffer is connected to a totem pole drive circuit for driving a common electrode with a high voltage which is synchronized with the logic signal. None of the references either singularly or in combination, teaches or fairly suggests: "The driving circuit for an organic EL device, wherein the power peripheral unit includes: an input terminal providing an applying external voltage an external voltage to the DC-DC converter; an output terminal outputting the controlled DC voltage output from the DC-DC converter to the outside the chip; a first capacitor connected with the input terminal in parallel to minimize fluctuation of the input voltage; a second capacitor connected with the output terminal in parallel to minimize fluctuation of the controlled DC voltage; an inductor connected in series between the input terminal and the output terminal, for maintaining the external voltage applied to the DC-DC converter for a predetermined time; and a diode connected in series between

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the input terminal and the output terminal, for preventing a backward current from occurring".

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:00AM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance



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Date 2-25-2003

A handwritten signature in black ink, appearing to read 'Richard Hjerpe', with a stylized, sweeping flourish extending from the end.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes **incorporated** therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may **NOT** be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.